NEW CIRCUIT TECHNIQUES AND DESIGN METHODES FOR INTEGRATED CIRCUITS PROCESSING SIGNALS FROM CMOS SENSORS

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Abstract: The body of this thesis deals with the analysis and design of circuits from a system on chip CMOS imager. The main topics are related to the analog blocks interfacing the photodiodes, processing of the analog signals and noise sources in the analog path to the A/D converter. Minimizing noise in such applications it is an important and challenging goal for designers. A good signal to noise ratio will allow a good resolution at the system level and finally a better image. As result precautions must be taken from the very beginning of the design process in order to minimize noise sources generated in the analog blocks. One of the scopes of this thesis is to identify, analyze and recommend solutions for noise reduction in integrated circuits including array of CMOS sensors.

1. ANALYSIS OF CMOS SENSORS AND ANALOG BLOCKS PROCESSING DATA FROM PIXELS

1.1. CMOS Imager Description

A CMOS imager is comprised of an array of photodiodes surrounded by analog circuits for processing the signals. The sensors are usually called pixels and are placed in a matrix structure.

A first stage of amplifiers, one amplifier associated to each column, amplifies the signals from pixels in a single-end configuration and outputs the signals to a second stage.

The second stage of amplifiers multiplexes the column signals to one differential signal at the input of an A/D converter with a programmable gain amplifier.

The first stage of amplifiers uses a double sample technique to minimize fixed pattern noise from pixels and columns.

1.2. Functional Description of the CMOS Imager

There are multiple structures of a pixel. A 3T structure have been implemented due to advantages related to higher power supply rejection ratio, higher speed in reading pixel array, lower noise in pixel and reduced fixed column pattern noise.

Some disadvantages are associated with this structure: reduced fill factor, large size of pixel, relatively complicated circuit to access pixel, fixed pixel pattern noise, reduced voltage range as result of presence of a source follower.

The figure 1.1 below shows two similar techniques, double sampling (DS) and correlated double sampling (CDS).
In applications needing image capture sometime the system works at different levels of ambient light. The level of ambient light can have a big impact on image quality in image recognition systems. As result a special circuit has been dedicated to measure the ambient light and send the signals to a processor in order to adjust the gain the analog path.

A separate array of photodiodes located at the periphery of the imager and monitored by a low resolution A/D converter allows the system to control the gain [1].

2. SWITCHED CAPACITOR AMPLIFIERS IN PIXEL DATA PROCESSING

2.1. Circuits in Switched Capacitor Amplifiers

The basic circuits in switched capacitor amplifiers are represented by CMOS switches, capacitors and operational amplifiers.

In a good process an error of about 0.1% is due to the capacitor mismatch. To keep the total error within this range the ON resistance of the CMOS switch charging a capacitor is given by:

\[ R_{on} \cdot C \leq T/20 \]  

where \( T \) is the switching period.

In designing switches, a few things must be considered:

- \( R_{on} \) could be decreased by increasing \( W/L \) but charge injection will increase;

- \( R_{on} \) is dependant on input voltage; some non-linear distortion should be taken into consideration;

- \( R_{on} \) is dependant on temperature (\( \mu, V_{th} \)) and process (\( C_{ox}, \mu, V_{th} \)).

Non-ideal characteristics of operational amplifiers such as offset, finite open loop gain, finite bandwidth, slew rate, output impedance should also be considered in design.

As general rules to follow:

- \( f_u \geq 5 \cdot f_c \);

- \( SR \geq 20 \cdot \omega_{max} \cdot V_{max} \);

where unity gain frequency of the opamp, switching frequency, slew rate, frequency and amplitude of the input signal have been considered [2].

2.2. Circuit Techniques for Switched Capacitor Amplifiers

The main sources of errors for CMOS opamps are offset and 1/f noise [2].

A double sampling technique is presented in this thesis. The circuit is based on a switch capacitor amplifier with offset compensation showed in the figure below.

The gain is given by:

\[ A_v = \frac{V'_o}{V_i} = \frac{A}{1 + A a}, \quad \frac{C_1}{C_2} = A \]
At low frequencies (signals not changing during two clock sequences) the error due to the open loop gain is proportional to 1/a. This technique will also compensate 1/f noise which is a low frequency noise [2].

3. NOISE AND NOISE REDUCTION IN INTEGRATED CIRCUITS WITH ARRAY OF CMOS SENSORS

3.1. Photodiode Temporal Noise

An analysis of the temporal noise could be done assuming that steady state is achieved when pixel is in reset mode [3].

Figure 3.1 presents a noise equivalent circuit of the pixel in reset.

The average reset power noise in reset can be estimated as:

$$v_{n_{fdz,r}}^2 = \frac{kT}{C_0} \quad (3.1)$$

In integration shot noise is dominant and assuming a constant capacitance of the photodiode, the noise voltage at the end of integration is given by:

$$v_{n_{fdz,i}}^2 = \frac{2q(I_N + I_S)}{C_0^2} \cdot t_{int} \quad (3.2)$$

and is it generated by two components: dark current and photodiode current [3].

3.2. Dark Fixed Pattern Noise

A simplified schematic of the CMOS sensor is presented below.

![Fig. 3.2. CMOS Sensor and Timing Diagram](image)

When double sampling is used the value at the end of integration is subtracted from the reset value and the result is a change in signal:

$$\left| \Delta V_{fd} \right| = \frac{(I_N + I_S) \cdot t_{int}}{C_0} \quad (3.3)$$

It can be seen that the errors are generated by dark current which can not be compensated, variations of the capacitance of photodiode and integration time.

3.3. Pixel Fixed Pattern Noise

This type of noise is due to mismatch of the source follower inside the pixel.

Figure 3.3 below shows a simplified circuit of the pixel and column biasing circuit. M3 is assumed closed (ON).

The output voltage is given by:
In a system with double sampling only the mismatch of transistors is important. Mismatch between biasing currents generates different gain for the source followers and as result a fixed column pattern noise.

3.4. Column Fixed Pattern Noise

One of the components of this type of noise has already been mentioned previously. Other errors will be generated in the operational amplifier used to process signals from pixels, in particular by offset and open loop gain.

Double sampling reduces the error due to offset and for open loop gain greater than 60 dB the closed loop gain is:

\[
A_v = A = \frac{C_1}{C_2}
\]  

(3.5)

As result the error is within the level of capacitor mismatch (0.1%) and in most cases can be ignored.

3.5. Dark Current Compensation

Dark current present at the pixel level cannot be compensated by using double sampling because it is not included in the RESET value generated by pixel [4].

In order to compensate dark current a special array of pixels located at the periphery of the imager is read in the same manner as active pixels. The signals from these dark columns are averaged and the resulting voltage is subtracted from the active signal in the second stage of amplifiers.

4. APPLICATIONS IN CMOS IMAGER

4.1. Programmable gain amplifier for pixel column

- Programmable gain: 1, 3, 5;
- Open loop gain: 70dB typical;
- Slew rate: minimum s / V 130 µ;
- Unity gain frequency: 220MHz typical.

4.2. Differential amplifier for black (dark) level compensation

- Gain programmable in two steps (1 and 2);
- Settling time within 0.1%: maximum 20ns;
- Sampling time: 10 clocks;
- Hold time: 1 clock cycle;
- Open loop gain: minimum 60dB;
- Unity gain frequency: minimum 150MHz.

4.3. Bandgap Reference

- Trimmed output: 6 bits;
- Temperature coefficient: maximum 40 ppm/oC;
- Current consumption: maximum 20µA;
- Settling time at power up: maximum 600µs.

CONCLUSIONS

Designing analog blocks for an integrated circuit including an array of CMOS sensors is a complex process and a challenge. Market research, defining final application, defining chip architecture must be important steps to be considered before the actual design process starts.

A complex chip such as an imager has a complex structure and functionality and DFT and DFR techniques have to be considered from the very beginning of the design.

On the analog block a careful analysis must be performed to identify all noise sources and minimize them. Auto zeroing techniques (double sample in particular) are necessary in order to compensate offset and 1/f noise. Some other techniques for minimizing thermal noise, charge injection, fixed pattern noise, substrate and power source noise have to be investigated and implemented.

If ambient light control is needed a special analog block has to be integrated in the imager to measure light and allow a processor to adjust the gain in the analog path.
5. CMOS IMAGER

5.1 Pictures of the Imager Designed by the Team Which the Author Was Part Of.

Die Top View

Packaged Imager Top View

5.2 CMOS Imager Characteristics

- Supply Voltage: 5V;
- Sensor Array: 1280x1024;
- Effective System Resolution: 8.5 bits;
- Gain: programmable in two stages from 1 to 25;
- Fill factor: 45%;
- Ambient light detection.

REFERENCES


