A FREQUENCY SYNTHESIZER STRUCTURE BASED ON COINCIDENCE MIXER

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Abstract: A frequency synthesis is a combination of electrical system elements that results in the generation of one or many frequencies from one or a few reference sources. The fine frequency resolution, low spurious signals, accuracy and stability are most important for these devices. The frequency synthesizers are an essential part of any modern communication system. They generate clock and oscillator signals needed for up and down conversion. In this paper, some new principles for synthesizers are described.

INTRODUCTION

Frequency synthesizers are an essential part of any modern transceiver system. They generate clock and oscillator signals needed for up and down conversion. Today’s communication standards demand both high frequency accuracy and fast frequency settling. Several different frequency synthesis techniques have been presented in the literature over the years. They can be quite clearly divided into three separate categories, namely direct analog synthesis, direct digital synthesis, and indirect analog synthesis. In this context, “indirect” refers to a system based on some kind of a feedback action, whereas “direct” refers to a system having no feedback [1].

1. A FREQUENCY SYNTHESIZER ARCHITECTURES

In direct analog synthesizer the frequency resolution is achieved by mixing signals of certain frequencies, and then dividing the resulting frequency down. Theoretically, this process can be repeated arbitrarily many times to achieve a finer frequency resolution. Advantages of the direct analog synthesis are very fast switching times and, in theory, arbitrarily fine frequency resolution. However, this technique requires a very large amount of hardware. Also, noise is a problem in direct analog synthesis. To achieve a reasonably low-noise output signal, all input frequencies will have to be low-noise crystal oscillators, resulting in a lot of external components. Moreover, all the mixers, bandpass filters, and dividers are in the signal path, meaning that their noise will also contribute to the phase noise in the synthesized frequency. The block diagram of a direct analog frequency synthesizer is shown in Fig. 1.

![Fig. 1. The block diagram of a direct analog frequency synthesizer. GEN - generator, MIX - mixer, FILT - bandpass filter.](image)

The second category is based on direct digital synthesis principle [2]. The block diagram is shown in Fig. 2. The desired output frequency is fed to the phase accumulator as a digital word.
The phase accumulator increments its output value by this word once every clock cycle. When the full scale of the accumulator is reached, it wraps around. The output of the phase accumulator is thus a digital ramp signal, whose period is the same as that of the desired output frequency. In other words, the phase accumulator output contains information about the instantaneous phase of the synthesized frequency.

![Fig. 2. The block diagram of a direct digital synthesizer. a) PHA - Phase accumulator, b) Phase to amplitude converter, c) D/A converter, d) Analog low-pass filter, M - input number, \( f_s \) - sampling (clock) frequency.](image1)

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The amplitude of a sinusoidal signal at different phase values is stored in the sine read-only memory (ROM). The instantaneous phase of the desired output signal is used as the address to the ROM, and the output is the instantaneous amplitude of the synthesized signal. To get an analog output signal, the amplitude information has to be converted to the analog domain in the digital-to-analog converter (D/A). The output of the D/C contains a lot of spurious tones (Fig. 3), harmonics, etc., that have to be filtered out before the signal can be used. The smoothing filter in the output of the D/C attenuates the harmonics to an acceptable level, but the in-band spurious tones still remain. Their frequencies are predictable, but as they are in the signal band, they will not be attenuated by the filter.

Direct digital synthesis has some very strong advantages. It has arbitrarily fine frequency resolution and a very high switching speed. Also, different phase, frequency, and amplitude modulations can be implemented in the digital domain, and require only a small amount of extra hardware. Due to the fact that most of the signal processing is done in the digital domain, direct digital synthesis also lends itself very well to full integration in a CMOS or BiCMOS technology.

![Fig. 3. Spectral analysis of sampled output (DDS D/A converter), example for \( f_{out} = 0.3 f_s \).](image2)

Fig. 3. Spectral analysis of sampled output (DDS D/A converter), example for \( f_{out} = 0.3 f_s \).

The last category are an indirect analog synthesizers or the phase-locked loop (PLL) shown in Fig. 4. Here, the synthesis is based on the feedback action of the loop [3]. The output frequency is divided down in the frequency divider. The phase of the output signal of the divider is compared with the phase of a reference signal in the phase detector. The output of the phase detector is lowpass filtered to generate a control voltage for the voltage-controlled oscillator (VCO). If the phase of the frequency divider output lags the phase of the reference frequency, the phase detector steers the VCO to a higher frequency, and vice versa. Indirect analog synthesis, or the phase-locked loop, is the most suitable technique for the synthesis of high-frequency sinusoidal signals. No block has to operate at a frequency higher than the output frequency. In addition, the only component that is necessarily external is the reference frequency oscillator (or at least the crystal used as the resonator in the oscillator).

![Fig. 4. The block diagram of phase-locked loop. VCO - voltage controlled oscillator.](image3)

Fig. 4. The block diagram of phase-locked loop. VCO - voltage controlled oscillator.
reference frequency. On the other hand, the loop bandwidth has to be significantly lower than the reference frequency, which results in relatively slow switching. Thus, the finer the frequency resolution of the PLL, the slower the switching speed. In addition to the three basic synthesis techniques introduced above, several modifications or combinations of them have been published [4]. Most of these synthesizers are modifications of the PLL, aiming to allow a wider loop bandwidth and a finer frequency resolution than the basic principle. Another proposed hybrid solution is generating the reference frequency of the phase-locked loop by a direct digital synthesizer. The DDS allows a fine frequency resolution while the bandwidth of the PLL is relatively large. However, all the spectral impurities in the output of the DDS will appear in the output of the synthesizer multiplied by the loop division ratio. Thus, the output of the DDS must be bandpass filtered, adding to the synthesizer’s complexity. Examples of amplitude disturbances in DDS are shown in Fig. 5 and 6.

2. FINE-STEP SYNTHESIZER

For fine-step frequency synthesizer the different schemas can be roughly organized into three classes: multi loop, fractional and direct digital synthesizers. Multi-loop architectures can provide clean output signal at the cost of complexity, physical size, and, in certain cases, of frequency hopping speed. Complex hardware implementations are typical and large dividers are not uncommon. Fractional synthesizers [5-8] provide fine frequency resolution and fast hopping with low complexity hardware, but they suffer from spurious signals very close to the carrier due to their inherent weak FM modulation. Direct digital synthesis (DDS) [2] (or numerical oscillators) is a convenient approach to fine step, large range, and fast hopping frequency synthesis using standardized building blocks. In almost all cases, the output signal is not purely periodic because of truncation errors generated in the phase accumulator and the digital-to-analog converter. This results in spurious signals very close to the carrier [2]. The general spectral purity is also limited by the digital-to-analog converter.

In this paper frequency synthesizer is based on programmable dividers, multipliers (based on PLL) and coincidence mixers. For this architecture, Cantor series approximations and Diophantine equations theory are used [9].

Let \( N_1, N_2, \ldots, N_k \) be relatively prime positive integers (GCD - Greatest common divisor of \( N_1, N_2, \ldots, N_k = 1 \)). Then for every integer \( u \), there exist a \( k \) integers \( X_1, X_2, \ldots, X_k \), solving the linear Diophantine equation:

\[
\frac{X_1}{N_1} + \frac{X_2}{N_2} + \ldots + \frac{X_k}{N_k} = \frac{u}{N_1/N_2/\ldots/N_k} \quad (1)
\]

If \( N_1, N_2, \ldots, N_k \) are relatively prime positive integers, then for every integer \( u \) such that:

\[
N = N_1 N_2 \ldots N_k
\]

Fig. 5. DDS output wave for \( \sin(2\pi 260k/1024) \)

Fig. 6. DDS output wave for \( \sin(2\pi 202k/1024) \)

Fig. 7. Optimal values of \( X_1, X_2, \ldots, X_k \) for example 1 and \( u = 0, 0.2 > /N_1 N_2 N_3 \)
The equation (1) has a solution \((X_1, X_2, \ldots, X_k)\), where that \(-N_i \leq X_i \leq N_i\) for all \(i=1,2,\ldots,k\).

It is important to say, that equation (1) has a \(k\) solutions (for \(-N_i \leq X_i \leq N_i\)).

**Example 1:**
\(N_1=7, N_2=9, N_3=11\) and \(u=1\). The solutions of (1) are shown in Tab. 1.:

<table>
<thead>
<tr>
<th>(X_1)</th>
<th>(X_2)</th>
<th>(X_3)</th>
<th>Sum</th>
</tr>
</thead>
<tbody>
<tr>
<td>-6</td>
<td>2</td>
<td>7</td>
<td>89</td>
</tr>
<tr>
<td>1</td>
<td>-7</td>
<td>7</td>
<td>99</td>
</tr>
<tr>
<td>1</td>
<td>2</td>
<td>-4</td>
<td>21</td>
</tr>
</tbody>
</table>

**Tab. 1.** Example of solution (1) for \(N_1=7, N_2=9,\) \(N_3=11\) and \(u=1\). Solution \([1, 2, -4]\) is optimal.

In Tab. 1., numbers in column 4 are computed as:

\[
\text{Sum} = \sum_{i=1}^{k} \frac{X_i^2}{N_i} \tag{2}
\]

and minimal value is optimal according eq. (2). Therefore, example 1 has solutions:

\[
\left(1/7\right)+\left(2/9\right)+\left(-4/11\right) = \left(-6/7\right)+\left(2/9\right)+\left(7/11\right) =
\left(1/7\right)-\left(7/9\right)+\left(7/11\right)\]
\(=1/(7*9*11)=1.443 \times 10^{-3}\)

**Example 2:**
\(N_1=7, N_2=9, N_3=11\) and \(u=10\). The optimal solution of (1) is: \([-4, 2, 4]\) (also \([3, -7, 4]\) and \([3, 2, -7]\)). Optimal values of \(X_1, X_2, X_3\) for example \(N_1=7, N_2=9, \) \(N_3=11\) and \(u=0, 0.2>-\)/\(N_1, N_2, N_3\) are shown in Fig. 7.

For frequency synthesizer consist of \(k\) dividers and multipliers the minimal frequency and minimal frequency step is given by (3):

\[
\text{Frequency step} = f_{REF} \frac{x}{k} \prod_{i=1}^{k} N_i \tag{3}
\]

for example 1, \(\text{Frequency step}=1.443 \times 10^{-3} f_{REF}\).

The hardware implementation part of \((X/N)\) is shown in Fig. 8. This can be simplified according Fig. 9. Output frequency is given by (4):

\[
f_{OUT} = \frac{X_i}{N_i} f_{REF} \tag{4}
\]

where \(f_{REF}\) is input frequency and \(f_{OUT}\) is output frequency.

**Fig. 9.** Simplified block diagram of Fig. 8.

**Fig. 10.** Block diagram of synthesizer part

Synthesizer part block diagram is shown in Fig. 10. Output frequency if given by (5):

\[
f_{OUT} = \left(\frac{X_1}{N_1} + \frac{X_2}{N_2}\right) f_{REF} \tag{5}
\]

The block diagram of final version of frequency synthesizer with 3 \((X/N)\) blocks is shown in Fig. 11. Output frequency of this synthesizer (for 3 blocks \(X/N\)) is given by equation:

\[
f_{OUT} = \left(\frac{X_1}{N_1} + \frac{X_2}{N_2} + \frac{X_3}{N_3}\right) M_s M_5 f_{REF} \tag{6}
\]

Structure of synthesizer (Fig. 11) can be simply extended for more \((X/Y)\) block.

**Fig. 11.** Final version of frequency synthesizer with 3 blocks \((X/N)\). The blocks M4 and M5 are PLL which acts as multipliers and signal shape.

**Fig. 12.** Conventional analog mixer based on multiplication function with output filter.
3. COINCIDENCE MIXER

As a review, let’s look at an conventional analog mixer, which performs the function of multiplication between two inputs (Fig. 12). Analog mixing implements the following trigonometric identity:

\[ C = AB = \cos(2\pi f_a t) \cos(2\pi f_b t) = \]
\[ = \frac{1}{2} \left[ \cos(2\pi (f_a + f_b) t) + \cos(2\pi (f_a - f_b) t) \right] \]  
(7)

and filtered output \( D \) (depend on filter quality):

\[ D = \frac{1}{2} \left[ \cos(2\pi (f_a + f_b) t) \right] \]  
(8)

There are some problems with filtering when frequencies \((f_a + f_b)\) and \((f_a - f_b)\) are close each other and tuning filter when frequency changing. Therefore new coincidence mixer was developed. New coincidence mixer, time diagram is shown in Fig. 13.

\[ f_R = \text{abs}(f_1 - f_2) \]  
(10)

The output pulses are generated on signals a) and b) coincidences and for sum of frequencies condition:

\[ C_{\text{SUM}} = \frac{d}{dt} \text{Signal}_a \oplus \frac{d}{dt} \text{Signal}_b \]  
(11)

where \( \oplus \) represent EX-OR function and for difference of frequencies:

\[ C_{\text{DIFF}} = \text{NEG}(C_{\text{SUM}}) \]  
(12)

where \( \text{NEG} \) is logical negation. It is important to note, that signal derivation (eq. 11) has a logical value and therefore is possible used logical operations.

The first main advantage of this mixer is that no output filter is need and therefore it has a wide frequency bandwidth without any tuning. The second advantage is almost pure digital architecture (only comparator and derivation function are not pure digital).

The first drawback of this synthesizer is pulsed output and therefore PLL on output is need for recovery triangle or sine output. The second condition is: The same amplitude of input signals.

The simplified block diagram of coincidence mixer is shown in Fig. 14.

4. SIMULATION RESULTS

The new coincidence mixer described above was simulated in Matlab. Fig. 15 shows the block diagram of mixer and Fig. 16 and Fig. 17 are time diagrams for input frequency \( f_i = 1/8 \)
and \( f_2 = 1/4 \) where Fig. 16 is result for sum of frequencies and Fig. 17 is for difference of frequencies.

**CONCLUSIONS**

The frequency synthesizer and new frequency mixer based on signal coincidence was described in this paper. In addition, simulation results were presented. The coincidence mixer was patented in Czech Republic in 2006.

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